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Code No. : 21511 SP

VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD
B.E. (I.T.) II Year I-Semester Special Examination, September-2017

Digital Electronics and Logic Design

Time: 3 hours

Max. Marks: 70

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

1. What is the specialty of Gray code?
2. Explain the principle of duality with the help of example.
3. What is PAL?
4. Write a short notes on Priority encoder.
5. Define Propagation delay time and set up time.
6. Difference between Latches and Flip-flops.
7. Distinguish between Mealy and Moore models.
8. What is a Finite state machine?
9. Give the notations used in an ASM CHART.
10. State the different types of hazards in combinational circuits.

Part-B (5 × 10 = 50 Marks)

(All bits carry equal marks)

11. a) Simplify the Boolean switching function and obtain its realization using only NAND gates. $F(A,B,C,D) = \sum m(0,1,3,4,6,9,11) + \sum d(2,5)$.
b) Draw the multiple level NOR circuit for the following expression: $w(x+y+z)+xyz$.
12. a) Design a 3-to-8 line decoder.
b) Design a BCD to EXCESS-3 code converter.
13. a) Explain about Master-slave JK flip-flop with the help of Timing diagram.
b) Design a decade counter to count in Excess-3 code sequence?
14. a) Explain the State Minimization Procedure with the help of example.
b) Design a circuit that detects three or more consecutive 1's in a string of bits coming through an input line.
15. a) Explain in detail the elements of an ASM chart.
b) Explain Static and Dynamic hazards in digital circuit.
16. a) Derive the circuits for a 3-bit parity generator and 4-bit parity checker using odd parity bit.
b) Design a code converter that converts a decimal digit from the 8-4-2-1 code to 2-4-2-1.
17. Answer any *two* of the following:
 - a) Design a 4 bit synchronous binary down counter.
 - b) Explain salient features of ASM CHART.
 - c) Write about hazards and clock skew.

